REMARKS

Claims 1-29 are currently pending. Claims 1, 11 and 21 are in independent form.

Claims 2 and 15 have been amended. No new matter is introduced hereby.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Claim Objections

Responsive to the comments in the outstanding Office Action with respect to the objections raised against claims 2 and 15, Applicant has appropriately amended the claims to rectify certain informalities noted therein.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

Part I

Claims 1, 11-14, 19, 20, 22-24, and 28-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,516,362 to Magro et al. (hereinafter the *Magro* reference) in view of U.S. Patent Application Publication No. 2002/0009169 to Watanabe (hereinafter the *Watanabe* reference). The following comments were provided in connection with these §103(a) rejections:

In re claim 1, Magro taught a system [microcontroller M] for synchronizing a first circuit portion [CPU 104] operating in a first clock domain that is clocked with a first clock signal [clk cpu 106] and a second circuit portion [SDRAM controller 102] operating in a second clock domain that is clocked with a second clock signal [clk mem 110] [fig 2a; abstract], comprising:

- Means for generating a sync pulse signal [phase sync 206] based on occurrence of a coincident edge between a first and second clock signals [fig 3b; col. 8, ll 6-48; phase sync is generated when both clocks are in phase, i.e., coincident edge as shown in fig. 3b, in order for timing of communication to work properly].
- A clock synchronizer controller [SDRAM controller 102] operable to generate a plurality of control signals based on sync pulse signal [col. 6, l.54 - col. 7, l.5], said clock synchronizer controller including a sync adjuster [clock synchronizer logic 202] operable to re-position said sync pulse signal based on a coincident edge between said first and second clock signals defined in response to a skew between said first and second clock signals [fig. 4, 5; col. 8, l.39 - col. 10, l.49; phase sync is automatically re-positioned in response to skew since it is generated in the same domain in which the determination of the skew is derived], wherein a least a portion of said plurality of control signals [data start, data end, etc.] actuate data transfer synchronizer circuitry disposed between said first and second circuit portions [col. 7, l.52 - col. 8, l.5; col. 12, ll.29-50].

Magro did not discuss re-positioning the sync pulse based on a *new* coincident edge between the first and second clock signals defined in response to a skew between the first and second clock signals.

However, it would have been obvious to one of ordinary skill in the art to recognize that the sync adjuster can be modified to include a re-positioning of the sync pulse based on a new coincident edge between the first and second clock signals defined in response to a

skew between the first and second clock signals in order to improve system performance by further removing any skew possible in the communication process [Watanabe: paragraph 0012-0014].

In claim 11, Magro discloses a method of synchronizing data transfer operations between two circuit portions across a clock domain boundary [abstract]:

- Generating a secondary clock signal from a primary clock signal [pll 108], wherein said primary clock signal [clk cpu 106] is operable to clock a first circuit portion [cpu 104] and said secondary clock signal [clk mem 110] is operable to clock a second circuit portion [SDRAM controller 102] [fig. 2b].
- Generating a sync pulse signal [phase sync 206] based on occurrence of a coincident edge between said primary and secondary clock signals [fig. 3b; col. 8, ll.6-48; phase sync is generated when both clocks are in phase, i.e., coincident edge as shown in fig. 3b, in order for timing of communication to work properly].
- Adjusting said sync pulse signal to re-position it based on a coincident edge that is defined responsive to a skew between said primary and secondary clock signals [fig. 4, 5; col. 8, l.39 - col. 10, l.49, phase sync is automatically re-positioned in response to skew since it is generated in the same domain in which the determination of the skew is derived].
- Generating data transfer control signals at appropriate times relative to said primary and secondary clock signals [col. 7, ll.59-66; col. 12, ll.33-50] based on said sync pulse signal [col. 9, ll.53-67] to control data transfer operations between said first and second circuit portions.

Magro did not discuss re-positioning the sync pulse based on a *new* coincident edge between the first and second clock signals defined in response to a skew between the first and second clock signals.

However, it would have been obvious to one of ordinary skill in the art to recognize that the sync

> adjuster can be modified to include a re-positioning of the sync pulse based on a new coincident edge between the first and second clock signals defined in response to a skew between the first and second clock signals in order to improve system performance by further removing any skew possible in the communication process [Watanabe: paragraph 0012-0014]. One of ordinary skill in the art would have been motivated to make such a modification as it provides a way to improve system performance [Watanabe: abstract].

Applicant respectfully traverses the foregoing §103(a) claim rejections and submits the following arguments as support. The present invention, as defined by the base claim 1, is directed to a system for synchronizing a first circuit portion operating in a first clock domain (clocked with a first clock signal) and a second circuit portion operating in a second clock domain (clocked with a second clock signal). A SYNC pulse signal is generated based on occurrence of a coincident edge between the first and second clock signals. A clock synchronizer controller is provided for generating a plurality of control signals based on the SYNC pulse signal, which clock synchronizer controller includes a SYNC adjuster operable to re-position the SYNC pulse signal based on a new coincident edge between the first and second clock signals that is defined in response to a skew between the clock signals.

In a further aspect, the base claim 11 is drawn to a method of synchronizing data transfer operations between two circuit portions

across a clock domain boundary. The method embodiment of claim 11 includes, *inter alia*, generating a SYNC pulse signal based on occurrence of a coincident edge between primary and secondary clock signals, and adjusting the SYNC pulse signal to re-position it based on a new coincident edge that is defined response to a skew between the clock signals.

Similarly, the method embodiment of base claim 21 involves generating a SYNC pulse signal based on occurrence of a coincident edge between a primary clock signal operable with a first clock domain and a secondary clock signal operable with a second clock domain, wherein skew compensation is based on (i) determining a state indicative of a phase difference between the primary and secondary clock signals, and (ii) redefining a new coincident edge with respect to the primary and secondary clock signals based on the state.

In contrast, the *Magro* reference does not teach or suggest generating a SYNC pulse signal based on occurrence of a coincident edge between two clock signals. Also, it does not teach or suggest a SYNC adjuster operable to re-position the SYNC pulse signal based on a new coincident edge between the two clock signals that is defined in response to a skew between the clock signals. More specifically, the *Magro* reference teaches a synchronization signal

called phase_sync signal 206 that is generated when the rising edge of a delayed slow clock signal, i.e., clk_cpu clock signal 106, always lags behind the corresponding rising edge of the faster clock signal, i.e., clk_mem clock signal 110. See FIG. 3a and FIG. 3b; see also col. 8, lines 6-38. Further, because the phase_sync signal 206 is generated within the faster clock domain, i.e, in the clk_mem frequency domain, the phase_sync signal 206 exhibits the same skew as the clk_mem clock signal 110. There is absolutely no teaching or even a scintilla of suggestion in the *Magro* reference with respect to adjusting the phase_sync signal 206 in order to re-position it based on a new coincident edge between the clk_mem and clk_cpu signals.

Further, the critical deficiency of the *Magro* reference as applied to the base claims 1, 11 and 21 is not cured by the secondary reference, i.e., the *Watanabe* reference, when combined as a basis for obviousness in the pending Office Action. It is well known that to establish obviousness, three basic criteria must be met. First, there must be some suggestion or motivation to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the combined references must teach or suggest all the claim limitations. See MPEP §2143. Applicant respectfully contends that there is no

suggestion or motivation in either of the applied references to combine the teachings therein so as to achieve the claimed invention directed to a solution where a SYNC adjuster mechanism is provided for re-positioning a SYNC pulse signal based on a new coincident edge between first and second clock signals that is defined in response to a skew between the clock signals. In contrast, the *Watanabe* reference is concerned with phase differences between parallel data channels. Specifically, *Watanabe* discloses a skew correction apparatus for making the deskew work possible even during the transmission of data in a data transmission system (see, e.g., paragraphs [0012] and [0013]), wherein skew amount constitutes a phase difference within different data transmission channels disposed between a transmitter 51 and a receiver 52 (see FIG. 5; see also paragraph [0066]). The skew correction apparatus of *Watanabe* includes a first skew correction means 31 for correcting the skew in the data channels during the idle time when no data is transmitted, and a second skew correction means 32 for correcting the skew during the data transmission after correcting the skew by the first skew correction means. See paragraph [0013]; see also FIG. 3. As provided at paragraph [0050], a primary skew correction circuit 42 (see FIG. 6) is included in the deskew circuit 522 (shown in FIG. 5), which

includes a maximum delay circuit 60 for selecting maximum delay signal from data 0 to data 3 (which constitute the receiving data in four exemplary channels), first variable delay circuits 610 to 613 for variably delaying the receiving data, phase comparator/voltage converters 620 to 623, digital converters 630-613 and an AND gate 64. With respect to the operation of the phase comparators, phase difference between the "0" position of an additional bit A in the signal output from the variable delay circuits 610 to 613 and the "0" position of the bit A in the most delayed data channel signal is detected by the phase comparators, and the particular phase difference is converted into a voltage difference that is applied to the variable delay circuits 610 to 613. See paragraph [0066]. Similar to the primary skew correction correct 42, the secondary skew correction means 32 (shown in FIG. 7) also includes variable delay circuits (delay adjust circuits) 651 to 653 for receiving the outputs of the variable delay circuits of the primary skew correction circuit 42. See paragraph [0051].

Applicant respectfully submits that neither of the skew correction means of the *Watanabe* reference even remotely relates to generating a SYNC pulse based on occurrence of a coincident edge between two clock signals, let alone re-positioning such a SYNC pulse signal based on a new coincident edge therebetween. As set

forth in detail hereinabove, the phase_sync signal 206 of the *Magro* reference is generated only when the rising edge of clk_cpu clock signal 106 is always behind the corresponding rising edge of clk_mem clock signal 110. The teachings of the *Watanabe* reference, however, do not shed any light with respect to adjusting the phase_sync signal 206 in order to re-position it based on a new coincident edge between the clk_mem and clk_cpu signals. Even if the teachings of the *Magro* and *Watanabe* references were to be combined somehow, it is respectfully contended that there is no reasonable expectation of achieving an operable result because of the inherent requirement that the phase_sync signal 206 be generated only when the rising edge of clk_cpu clock signal is behind the corresponding rising edge of clk_mem clock signal, which teaches away from generating a SYNC pulse signal based on occurrence of a coincident edge between two clock signals as currently claimed.

Accordingly, Applicant respectfully submits that claims 1, 11-14, 19, 20, 22-24, and 28-29 are patentable over the *Magro* and *Watanabe* references.

Part II

In the pending Office Action, claims 15-17, 21, and 25-26 are rejected under 35 U.S.C. §103(a) as being unpatentable over the

Magro and *Watanabe* references as applied above, and further in view of U.S. Patent No. 6,212,249 to Shin (hereinafter the *Shin* reference). The following comments were provided with respect to the *Shin* reference:

> Shin discloses a method of synchronizing data transfer operations between two circuit portions [abstract], comprising:
>
> - Determining a state [I-III] indicative of a phase difference between a primary [reference clock] and secondary [window signal] clock signals [col. 6, l.45 - col. 7, l.19].
> - Redefining a new coincident rising edge with respect to the primary and secondary clock signals based on the state [col. 7, l.30 - col. 9, l.3].
>
> It would have been obvious to one of ordinary skill in the art, having the teachings of Magro, Watanabe, and Shin before him at the time of the invention, to modify the system taught by Magro and Watanabe to include the teaching of Shin in order to obtain the method comprising determining a state indicative of a phase difference between a primary and secondary clock signals and redefining a new coincident rising edge with respect to the primary and secondary clock signals based on the state. One of ordinary skill in the art would have been motivated to make such a modification as it provides a way to maintain system stability [Shin: col. 2, ll.7-37].

Applicant respectfully traverses the foregoing §103(a) rejections and submits the following arguments as support. As discussed above, the combination of the *Magro* and *Watanabe* references is of no avail in terms of providing a proper basis for the §103(a) rejection of the base claims 11 and 21. Application of

the *Shin* reference does not cure this deficiency, however. *Shin* discloses a data separation circuit and method for a floppy disk controller in which the data rate with which the data is read from the floppy disk may increase (i.e., a fast state) or decrease (i.e., a slow state). Col. 5, lines 7 - 17. A window signal (FIG. 3C) is employed that includes a data area and a clock area for dividing read data bits and clock pulses from a common read data stream. Col. 4, line 58 to col. 5, line 6. For proper operation, the window signal must also change as the data rate changes. Col. 5, lines 17 - 21.

As shown in FIG. 2, the data separation circuit of *Shin* includes a digital phase-locked loop (DPLL) 29 that outputs the window signal. Output of MUX 24 serves as a reference clock for DPLL 29. A phase detecting part 25 is provided for detecting a phase error between the reference clock and the window signal. In operation, the phase detecting part 25 outputs a first and second error signal wherein the first error signal indicates phase error in a first direction and the second error signal indicates phase error in a second direction opposite to the first direction. Col. 4, lines 13 - 25. FIG. 6 in the *Shin* reference depicts how the phase detecting part 25 produces the first and second error signals indicative of phase error in one or the other directions by

determining a phase difference state between the reference clock and window signal. Responsive to the first and second error signals, a phase/frequency controlling part 26 generates a control signal to a digital control oscillator 27.

The purpose of the digital control oscillator 27 is to lock the frequency of the window signal to the reference clock such that even when the data rate with which data is read from the floppy disk changes, a corresponding change in the window signal is achieved. As a result, the data separation circuit can continue to generate a data signal and a clock signal from the delayed read data signal. Col. 8, line 63 to col. 9, line 3. Accordingly, although DPLL 29 operates to increase or decrease the length of time between pulses in the window signal in accordance with changes in data rate based on the reference clock, it does not generate a separate SYNC pulse based upon occurrence of a coincident edge between the window and reference clock signals. Further, the phase difference states determined by the phase detecting part 25 do not suggest or allude to redefining a new coincident edge between two clock signals based on the determined state. Nor do the phase difference states relate to adjusting a SYNC pulse signal in response thereto.

Applicant respectfully submits that there is no suggestion or motivation in any of the applied references to combine the teachings therein so as to achieve the claimed invention directed to a solution where a SYNC adjuster mechanism is provided for re-positioning a SYNC pulse signal based on a new coincident edge between first and second clock signals that is defined in response to a state indicative of a phase difference. On the other hand, even if the teachings of the *Magro* and *Watanabe* references were to be combined somehow with the teachings of the *Shin* reference, it is respectfully contended that there is no reasonable expectation of achieving success because of the inherent requirement that the phase_sync signal of the *Magro* reference be generated only when the rising edge of clk_cpu clock signal is behind the corresponding rising edge of clk_mem clock signal (i.e., with a fixed phase relationship), which teaches away from variable phase differences in either direction between the reference clock and window signals as disclosed in the *Shin* reference.

Accordingly, Applicant respectfully submits that claims 15-17, 21, and 25-26 are patentable over the *Magro*, *Watanabe* and *Shin* references.

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Part III

In the outstanding Office Action, claim 18 and 27 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Magro* reference (as applied to the base claims 11 and 21 above) in view of U.S. Patent No. 5,987,081 to Csoppenszky et al. (hereinafter the *Csoppenszky* reference). The following comments were provided in connection with these §103(a) rejections:

> Magro taught a synchronizer for transferring data between two different clock domains by generating various data transfer control signals [col. 6, ll. 64-66] for the data transfer synchronizer circuitry [130] disposed between the first and second circuit portions [Fig. 2b].
>
> However, Magro did not disclose expressly the details of configuration in which the data transfer control signals are transferred.
>
> Csoppenszky taught a synchronizer for data transfer between clock domains [abstract], the synchronizer comprising of data transfer control signals that are staged through a plurality of registers [col. 6, ll. 7-36].
>
> An ordinary artisan at the same time the invention was made would have been motivated to look for a stable way to transfer data in a system with two different clock domains [Csoppenszky: col. 1, ll. 11-45].
>
> Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Magro and Csoppenszky because of the aforementioned motivation and also their involvement in similar problems regarding the synchronization of data transfer in a two-clock domain system.

Applicant respectfully traverses the pending §103(a) rejections in view of the arguments set forth in the foregoing discussion. As discussed above with respect to the base claims 11 and 21, the *Magro* reference does not suggest or even remotely allude to the claimed limitations of generating a SYNC pulse signal based on occurrence of a coincident edge between two clock signals and adjusting the SYNC pulse signal to re-position it based on a new coincident edge that is defined responsive to a skew between the two clock signals. Applicant further submits that reliance on the *Csoppenszky* reference is of no avail in this regard. The *Csoppenszky* reference is directed to a method and apparatus for deterministically transferring data across an asynchronous boundary in a test environment. Col. 2, lines 40-42. A synchronizer comprising a series of flip-flops is provided for effectuating data transfer from one clock domain to a second clock domain operating at a higher clock frequency. Col. 2, lines 43-46. A clock enable signal is defined so as to approximately align the enabled rising edges of the faster clock signal with the falling edges of the slower clock signal. This approximate alignment provides a timing window of one half period of the slower clock for the data to stabilize at the input of a flip-flop in the faster clock domain before it is sampled. Col. 2, lines 54-57.

Applicant respectfully contends that there is no suggestion or motivation in either of the applied references to combine the teachings therein so as to achieve the claimed invention wherein a SYNC pulse signal is generated based on occurrence of a coincident edge between two clock signals, which SYNC pulse signal is operable to be adjusted so as to re-position it based on a new coincident edge that is defined responsive to a skew between the two clock signals. In addition, the combination of the *Magro* and *Csoppenszky* references fails to teach or suggest all of the limitations of the present invention as currently claimed. Accordingly, Applicant respectfully submits that claims 18 and 27, which are dependent from the base claims 11 and 21, respectively, are patentable over the applied combination of the references.

Regarding the Allowable Subject Matter

Applicant gratefully appreciates the indication in the pending Office Action that claims 2-10 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In view of the present response, it is believed that claims 2-10 are in condition for allowance in their current form.

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SUMMARY AND CONCLUSION

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding rejections and allow claims 1-29 presented for reconsideration herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested.

Respectfully submitted,

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Shreen K. Danamraj
Registration No. 41,696

DANAMRAJ & YOUST, P.C.
Premier Place, Suite 1450
5910 North Central Expressway
Dallas, Texas 75206
Tel 214.750.5666
Fax 214.363.8177